# DRAGSTER DR-16k-3.5

# Product Flyer

Part name : DR-16k-3.5
Revision : 1.0
Date : 11- 09 - 2009

Design house : AWAIBA Lda.
Contact Address : CEIM Sala 4, Madeira Technopolo, 9020-105 Funchal, Madeira, PORTUGAL
Contact Phone : +351 291 723 124; +49 4102 457 176
Contact E-mail : info@awaiba.com

# 1 History Record

| Version | Date | Modifications | Author |
|---|---|---|---|
| 1.0 | 11.09.2008 | Document creation | M. Wäny |
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# 2 Contents

# 3 Introduction

DRAGSTER is a platform of a digital line-scan sensors. The Sensor family is organized such that line-scan sensor with basic elements of 1x 4k pixels respectively 2x 4k pixels with 3.5um pitch can be easily realized. E.g. sensors with pixel numbers of:

1x 4k; 1x 6k; 1x 8k; 1x 12k; 1x16k
2x 4k, 2x 6k; 2x 8k; 2x 12k; 2x 16k

Are possible. For all variations the basic readout and control electronics are identical.

The sensor features a low noise pixel with true CDS and global shutter for interleaved readout and integration operation. Each pixel has an on pixel ADC and 13bit readout register. AD conversion is made to 12.2 bits and for output clamped to 12bit to guarantee full 4096 DN signal swing. The ADC gain can be programmed in a range of -6dB till + 20 dB by means of an 8bit DAC controlled over the serial configuration interface.

The readout is made by 4 12bit wide digital taps organized in odd / even order for each 4k segment. (full 13 bit readout is possible for special purposes) For each line all 16k pixels have to be read out, as the minimum time for the AD conversion equals approximately the time for a full readout. For DR-16k-3.5 with a pixel clock of 50MHz a total pixel rate of 800Mpixel/s is obtained.

To enhance dynamic range multiple non destructive readouts are possible.

# 4 Electrical Description

## 4.1 Operating Conditions

Functional operation is guaranteed under these conditions.

| Symbol | Description | min | typical | max | unit |
|---|---|---|---|---|---|
| VDDD | Power supply voltage (digital) | 3.2 | 3.3 | 3.4 | V |
| VDDA | Power supply voltage (analogue) | 3.2 | 3.3 | 3.4 | V |
| VDD/IO | Power supply voltage (I/O) | 3.2 | 3.3 | 3.4 | V |
| VSSD | Ground supply (digital) | | 0 | | V |
| VSSA | Ground supply (analogue) | | 0 | | V |
| VSS/IO | Ground supply (I/O) | | 0 | | V |
| Fclk * | Input Clock Frequency | 1 | | 50 ** | MHz |
| Duty_clk | Input Clock Duty cycle | 45 | 50 | 55 | % |
| Jitter_clk | Input Clock Jitter | | | 100 | ps |
| Cload | Load capacitance on digital I/O's | | | 10 | pF |
| Tj | Junction temperature | 0 | 27 | +80 | °C |
| VnrmsVDDD | RMS Noise on VDD digital | | | 20 | mV |
| VnppVDDD | Peak to Peak Noise on VDD digital | | | 100 | mV |
| VnrmsVDDA | RMS Noise on VDD analogue | | | 5 | mV |
| VnppVDDA | Peak to Peak Noise on VDD analogue | | | 20 | mV |
| VnrmsVDD/IO | RMS Noise on VDD I/O | | | 20 | mV |
| VnppVDD/IO | Peak to Peak Noise on VDD I/O | | | 100 | mV |
| Vil | Low level input voltage | -0.3 | 0 | 0.4 | V |
| Vih | High level input voltage | 0.8*VDD/ | VDD/IO | VDD/IO | V |

| | | | | | |
|---|---|---|---|---|---|
| | | IO | | +0.3 | |

* Fclk can be lower then 1MHz however the ADC conversion accuracy might be reduced. ** the ADC can be clocked with up to 100MHz for faster conversion when using clock reduction for readout.

## 4.2 Electrical characteristics

| **Symbol** | **Description** | **Min** | **Max** | **Unit** |
|---|---|---|---|---|
| Vol | Low level output voltage | | 0.5 | V |
| Voh | High level output voltage | VDD/IO-0.6 | | V |
| Iil | Low level input leakage (Vi=0) | | +-1 | uA |
| Iih | High level input leakage (Vi=VDD/IO) | | +-1 | uA |
| tslew, rising | Output slew rate of rising edge* | | 2.5 | ns |
| tslew, falling | Output slew rate of falling edge* | | 2.5 | ns |
| Ptot** | Power Consumption | | 3200 | mW |
| I (VDDA) | Current to analog devices | | 400 | mA |
| I (VDDD) | Current to Digital devices | | 220 | mA |
| I (VDDIO) | Current for I/O | | 260 | mA |
| I (VDD_bulk) | Current over bulk contacts, nominal no DC current, should be designed to support equal current to VDDD | | | |
| I (VDDESD) | Current over bulk contacts, nominal no DC current, should be designed to support equal current to VDDD | | | |

* @ 10pF

** At VDDDIO = 3.3V 46MHz Cload dig 10pF 20% I/O activity

## 4.3 Optical characteristics

| Parameter | Min | Typ/ Target | Max | unit |
|---|---|---|---|---|
| Pixel Size x*y | | 3.5*3.5 | | um2 |
| Pixel Pitch x | | 3.5 | | um |
| Number of pixels | | 16448 | | pixels |
| Number of light sensitive pixels | | 16384 | | pixels |
| Fill Factor | | 100 | | % |
| Quantum efficiency at 630nm | 50 | 60 | 70 | % |
| Full Well capacity(4) | 15 | 23 | 35 | ke- |
| Total System Gain K | | 0.076 | | DN/e- |
| DSNU rms (1;5) | | 3 | 10 | DN/12bit |
| Responsivity (1) | | 39 | | DN/nJ/cm2 (@12bit) |
| Responsvity analogue gain 4x (6) | | 116 | | DN/nJ/cm2 (@12bit) |
| PRNU rms (1;5) | | 1 | 3 | % (full scale) |
| PRNU pp (1; 5) | | 4% | 8 | % (full scale) |
| ADC Programmable gain | -6 | | 20 | dB |
| ADC gain resolution | | 8 | | bit |
| Blooming overload tolerance | 100x | infinite | | |
| Lag | | 0 | 0.1 | % |
| Crosstalk (optical & electrical) | | 2 | 5 | % |
| Exposure time range | 2 | | infinite | us |
| Temporal noise Dark rms (2)* | | 2 | 4 | DN/12bit |
| Dark noise electrons rms (2) | | 26 | | e- |
| Dark noise electrons rms gain x4 (6) | | 13 | | e- |
| NEE (noise equivalent energy) unity gain (1) | | 0.04 | | nJ/cm2 |
| Temporal noise Dark rms gain 4x (6)* | | 3.6 | 5 | DN/12bit |
| NEE (noise equivalent energy) analogue gain x4 (6) | | 0.02 | | nJ/cm2 |
| Non Linearity (3) | | 2 | 5 | % |
| Dark current @27C | | 1 | 20 | e-/ms |
| Maximum Line Rate | | | 40 | kScan/s |

| Parameter | Min | Typ/ Target | Max | unit |
|---|---|---|---|---|
| ADC Resolution | | 12 | | bit |
| Number of output taps | | 16 (4per 4k segment) | | |
| Configuration Interface | | Serial 4 line | | |
| Integration control | | Asynchronous, with 6 digital signals | | |
| Trigger delay | | | 1 | us |
| Integration & Readout | | Interleaved | | |

(1) Tint=10us, Unity gain (CDS_gain = 0 -> x1; Inverse ADC gain = 0x10h)
(2) T=27ºC , Tint=20us, Unity gain (CDS_gain = 0; -> x1 Inverse ADC gain = 0x10h)
(3) Measured in % deviation from full scale signal for the signal range of 5% - 95% (according to EMVA1288 proposal for linearity measurement)
(4) At unity gain (CDS_gain = 0 -> x1; Inverse ADC gain = 10; end counter 128 (4096 ADC levels))
(5) Ramp offset and ramp gain must be adjusted for all segments to match with each other.

(6) T=27ºC , Tint=20us, Unity gain (CDS_gain = 1; -> x4 Inverse ADC gain = 0x10h)

* {info only: temporal noise can further be reduced by subtracting from each line the average value of the dark reference pixels, which will reduce temporal noise components coupled over the supply at frequencies below the line rate. :end info}